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APPLICATION FOR LETTERS PATENT

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Method of Forming Trench Isolation Regions

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INVENTORS

Trung Tri Doan
Gurtej S. Sandhu

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TECHNICAL FIELD

This invention relates to methods of forming trench isolation regions in semiconductive substrates.

BACKGROUND OF THE INVENTION

In modern semiconductor device applications, numerous devices are packed onto a single small area of a semiconductor substrate to create an integrated circuit. For the circuit to function, many of these individual devices may need to be electrically isolated from one another. Accordingly, electrical isolation is an important and integral part of semiconductor device design for preventing the unwanted electrical coupling between adjacent components and devices.

As the size of integrated circuits is reduced, the devices that make up the circuits must be positioned closer together in order to comply with the limited space available on a typical semiconductor substrate. As the industry strives towards a greater density of active components per unit area of semiconductor substrate, effective isolation between circuits becomes all the more important.

The conventional method of isolating circuit components in modern integrated circuit technology takes the form of trench isolation regions etched into a semiconductor substrate. Trench isolation regions are commonly divided into three categories: shallow trenches (STI) (trenches less than about 1 micron deep); moderate depth trenches (trenches of

from about 1 to about 3 microns deep); and deep trenches (trenches greater than about 3 microns deep). Once the trench isolation regions are etched in the semiconductor substrate, a dielectric material is deposited to fill the trenches. As the density of components on the semiconductor substrate increased, the widths of the trenches decreased until the process of flowing dielectric material into the trenches developed problems.

Trench isolation regions, particularly STI regions, can develop undesirable voids in the dielectric material during the process to fill the trenches. As the dielectric material flows to an edge between a substrate surface and a sidewall of the trench, constrictions develop at the top of trenches due to the narrow opening in the trench. As the dielectric material flows into the trench, the constrictions can develop into voids moving into the trench with the dielectric material. Voids lower the dielectric characteristics of the dielectric material used and introduce structural instabilities in subsequent processes. Accordingly, voids in the dielectric material filling an isolation trench region are highly undesirable.

SUMMARY OF THE INVENTION

In accordance with an aspect of the invention, a method of forming a trench isolation region includes forming a trench within a substrate. A silanol layer is formed to partially fill the trench and

then at least some of the silanol is converted to a compound comprising at least one of SiO_n and $RSiO_n$, where R comprises an organic group. An electrically insulative material is formed over the converted silanol to fill the trench.

In another aspect of the invention, a method of forming a trench isolation region includes forming a trench within a substrate. A first layer of at least one of $Si(OH)_x$ and $(CH_3)_ySi(OH)_{4-y}$ is formed to partially fill the trench. At least some of the $Si(OH)_x$ if present is converted to SiO_2 and at least some of $(CH_3)_ySi(OH)_{4-y}$ if present is converted to $(CH_3)_xSiO_{2-x}$. Next, a layer of an electrically insulative material is formed to fill the trench.

In yet another aspect of the invention, a method of forming a trench isolation region includes forming a trench within a substrate. The trench has sidewalls comprising silicon and a base comprising silicon. A first electrically insulative layer is formed over the sidewalls and base. The first electrically insulative layer is anisotropically etched to expose silicon of the base while leaving silicon of the sidewalls covered. A second electrically insulative layer is substantially selectively chemical vapor deposited over the exposed trench base. A third electrically insulative layer is formed over the first and second insulative layers to within the trench.

In still another aspect of the invention, a method of forming a trench isolation region includes forming a trench having sidewalls within

a substrate. The sidewalls are thermally oxidized in an oxidizing environment which includes oxygen and hydrogen with a greater molar concentration of hydrogen than oxygen. A layer of silanol is formed to within the trench and at least some of the silanol is converted to a compound of at least one of SiO_n and $RSiO_n$, where R includes an organic group.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Figure 1 is a fragmentary sectional view of a semiconductor substrate at one processing step in accordance with a first embodiment of the invention.

Figure 2 is a view of the Figure 1 substrate fragment at a processing step subsequent to that shown in Figure 1.

Figure 3 is a view of the Figure 1 substrate fragment at a processing step subsequent to that shown in of Figure 2.

Figure 4 is a view of the Figure 1 substrate fragment at a processing step subsequent to that shown in of Figure 3.

Figure 5 is a fragmentary sectional view of a semiconductor substrate at one processing step in accordance with a second embodiment of the invention.

Figure 6 is a view of the Figure 5 substrate fragment at a processing step subsequent to that of Figure 5.

Figure 7 is a view of the Figure 5 substrate fragment at a processing step subsequent to that of Figure 6.

Figure 8 is a fragmentary sectional view of a semiconductor substrate at one processing step in accordance with a third embodiment of the invention.

Figure 9 is a view of the Figure 8 substrate fragment at a processing step subsequent to that of Figure 8.

Figure 10 is a view of the Figure 8 substrate fragment at a processing step subsequent to that of Figure 9.

Figure 11 is a view of the Figure 8 substrate fragment at a processing step subsequent to that of Figure 10.

Figure 12 is a view of the Figure 8 substrate fragment at a processing step subsequent to that of Figure 11.

Figure 13 is a fragmentary sectional view of a semiconductor substrate at one processing step in accordance with a fourth embodiment of the invention.

Figure 14 is a view of the Figure 13 substrate fragment at a processing step subsequent to that of Figure 13.

Figure 15 is a view of the Figure 13 substrate fragment at a processing step subsequent to that of Figure 14.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

With reference to Figures 1-4, a method of forming a trench isolation region is illustrated. Referring to Figure 1, a semiconductor substrate fragment in process is indicated generally with reference numeral 10. Preferably, the semiconductor substrate fragment 10 comprises the following layers shown in elevationally ascending order: a semiconductor substrate 12, preferably a bulk monocrystalline silicon substrate; an oxide layer 20; and a silicon nitrite layer 22. A series of trenches 14 are formed, preferably by an etching process, through layers 20 and 22 and within semiconductor substrate 12. Trench isolation regions 14 have sidewalls 16 and base walls 18.

Referring to Figure 2, a first layer 26 is formed, and initially comprises a silanol which partially fills trenches 14. An exemplary method of forming the first layer 26 is as follows. SiH_4 and H_2O_2 are separately introduced into a chemical vapor deposition (CVD) chamber, such as a parallel plate reaction chamber (not shown). The reaction rate between SiH_4 and H_2O_2 can be moderated by the introduction of nitrogen into the reaction chamber. Semiconductive substrate 12 within the chamber is preferably maintained at a suitably low temperature, such as 0°C, at an exemplary pressure of 1 Torr to achieve formation of a

silanol-type material of the formula $Si(OH)_x$, which is predominately $Si(OH)_4$. The $Si(OH)_4$ condenses onto the semiconductor substrate 12 surface to form layer 26.

Alternatively, first layer 26 is formed to comprise $(CH_3)_ySi(OH)_{4-y}$ at least initially to partially fill the trench. The formation of $(CH_3)_ySi(OH)_{4-y}$ can be accomplished similarly to that described above for forming silanol, with the exception that $(CH_3)_2SiH_{4-z}$, wherein z is at least 1 and no greater than 4, is combined with the hydrogen peroxide (H_2O_2). For example, CH_3SiH_3 can be combined with H_2O_2 to produce $CH_3Si(OH)_3$.

Although either reaction occurs in the gas phase, the initially deposited first layer 26 ($Si(OH)_x$ or $(CH_3)_ySi(OH)_{4-y}$) is preferably in the form of a viscous liquid which preferably flows very conformably, ideally depositing over trench base 18 faster and thicker than over sidewalls 16. A preferred thickness for first layer 26 is at least 25% of the trench depth, and more preferably at least 35%, while preferably adding only 200 angstroms or less to sidewalls 16.

After forming first layer 26 over semiconductor substrate 12, at least some of it is converted to a compound comprising at least one of SiO_n and $RSiO_n$, where R comprises an organic group. An exemplary process for doing so is to treat first layer 26 with energy to drive water therefrom and convert to a silicon oxide comprising structure. A specific exemplary method of converting first layer 26 comprises exposing the first

layer 26 to ultraviolet light, with other examples of energy being electron beam energy or plasma, and RF energy. Preferably, a two-step process is employed. First, polymerization of the liquid film is promoted by increasing the temperature to above 100°C, while maintaining the pressure of about 1 Torr, to result in solidification and formation of a polymer layer. Thereafter, the temperature is raised to above 300°C, preferably above 400°C, while maintaining a pressure of about 1 Torr, preferably at least 10 atmospheres.

Referring to Figure 3, a second layer 30 is formed comprising an electrically insulative material, preferably silicon dioxide, over converted silanol layer 26 to within the trenches 14. Preferably as shown, second layer 30 is formed to fill remaining volume of trenches 14. An exemplary process for forming second layer 30 comprises chemical vapor deposition, preferably plasma-enhanced chemical vapor deposition. For example, conventional high density plasma deposited SiO_2 can be formed. In the context of this document, "high density" refers to a plasma having at least 10^{10} ions/cm^3 plasma density. An optional gettering process may be performed at this stage of the process.

Referring to Figure 4, planarization can be conducted (i.e., chemical-mechanical polishing) to remove layers 30, 22 and 20 from over the substrate outside of trenches 14.

With reference to Figures 5-7, another embodiment in accordance with the invention is described. Like numerals from the first described

embodiment are employed where appropriate, with differences being indicated with a suffix (a) or with different numerals.

Referring to Figure 5, a semiconductor substrate fragment in process is indicated generally with reference numeral 10a. An electrically insulating first layer 40 is chemical vapor deposited to within trenches 14 to partially fill the trenches. Preferably, first layer 40 comprises silicon dioxide (SiO_2) and fills at least 25% of the trench 14 depth. First layer 40 is preferably deposited by plasma-enchanced chemical vapor deposition, preferably by high density plasma or subatmospheric chemical vapor deposition.

Referring to Figure 6, a second layer 44 comprising a silanol is formed over first layer 40 to within trenches 14. Preferably, the method to form second layer 44 is by the same method previously discussed and disclosed for forming first layer 26 of the Figures 1-4 embodiment. Consequently, as with the previous method, second layer 44 preferably fills trenches 14, preferably is maintained at a temperature of at least about 300° C and at a pressure of at least about 10 atmospheres effective to drive water from second layer 44, and preferably is converted to a silicon oxide comprising structure by exposure to energy, for example ultraviolet light.

Referring to Figure 7, planarization can be conducted (i.e., chemical-mechanical polishing) to remove layers 44, 40, 22 and 20 from over the substrate outside of trenches 14.

With reference to Figures 8-12, yet another embodiment in accordance with the invention is described. Like numerals from the previously described embodiments are employed where appropriate, with differences being indicated with a suffix (b) or with different numerals.

Referring to Figure 8, a semiconductor substrate fragment in process is indicated generally with reference numeral 10b. An electrically insulative layer 21 is formed over silicon trench sidewalls 16 and trench base 18. An example thickness for layer 21 is 150 angstroms. A preferred material for layer 21 is silicon dioxide. An exemplary method of forming layer 21 comprises chemical vapor deposition, and alternatively thermal oxidation. An example thermal oxidation comprises flowing an oxidizing gas (i.e., O_2, O_3, N_2O, NO_X or any mixture combination thereof) over substrate 12 within trenches 14 while substrate 12 is maintained at from 850°C to 1150°C for from 5 to 30 minutes. An example chemical vapor deposition process comprises injecting tetraethylorthosilicate (TEOS) into a reactor chamber at 500 mg/min while flowing O_3, preferably as a mixture of 12% O_3 and 88% O_2, at 4000 sccm and helium at from 0-200 sccm and maintaining the substrate 12 at 550°C and reactor pressure at 200 Torr.

Referring to Figure 9, insulative layer 21 is anisotropically etched to expose silicon of the base walls 18 while leaving silicon of the sidewalls 16 covered. An exemplary anisotropic etch comprises a conventional oxide spacer etch.

Referring to Figure 10, a second electrically insulative layer 50 is substantially selectively deposited over the exposed base walls 18 to partially fill the trenches 14. Preferably, layer 50 comprises an oxide deposited by chemical vapor deposition, and more preferably silicon dioxide. An exemplary chemical vapor deposition to form layer 50 comprises liquid injecting TEOS into a reactor chamber at 350 mg/min while flowing O_3, preferably as a mixture of 12% O_3 and 88% O_2, at 5000 sccm and helium at from 0-200 sccm and maintaining the substrate 12 at 400°C and reactor pressure at 600 Torr.

Referring to Figure 11, a layer 30 is formed comprising an electrically insulative material, preferably silicon dioxide, over layers 21, 22 and 50 to within trenches 14. Preferably as shown, layer 30 is formed to fill remaining volume of trenches 14. An exemplary process for forming second layer 30 comprises chemical vapor deposition, preferably high density plasma-enhanced chemical vapor deposition as described above. An alternative method of forming layer 30 comprises flowing a silanol layer to fill within trenches 14. The method to form layer 30 is preferably by the same method previously discussed and disclosed for forming first layer 26 of the first embodiment shown in Figures 1-4 and second layer 44 of the second embodiment shown in Figures 5-7.

Referring to Figure 12, planarization can be conducted (i.e., chemical-mechanical polishing) to remove layers 30, 22, 21 and 20 from over substrate 12 outside of trenches 14.

With reference to Figures 13-15, still another embodiment in accordance with the invention is described. Like numerals from the first described embodiment are employed where appropriate, with differences being indicated with a suffix (c) or with different numerals. Referring to Figure 13, an electrically insulative layer 21 is formed over silicon trench sidewalls 16 and trench base 18 by a thermal oxidization process. An exemplary method of forming layer 21 comprises thermally oxidizing the sidewalls of the trench in an oxidizing environment comprising oxygen and hydrogen and having a greater molar concentration of hydrogen than oxygen. An example thermal oxidation comprises flowing an oxidizing gas at 200 sccm (i.e., O_2, O_3, N_2O, NO_X or any mixture combination thereof) and hydrogen source at 1 slm (i.e., H_2, NH_3 or any mixture combination thereof) over substrate 12 within trenches 14. Preferably, substrate 12 is maintained at from 800°C to 1100°C and reactor pressure at from 10 Torr to 760 Torr for from 1 to 20 minutes.

Referring to Figure 14, a silanol layer 44 is formed over layers 21 and 22 to within trenches 14. At least some of the silanol is converted to a compound comprising at least one of SiO_n and $RSiO_n$, where R comprises an organic group. The method to form layer 44 is preferably by the same method previously discussed and disclosed for forming first

layer 26 of the first embodiment shown in Figures 1-4 and second layer 44 of the second embodiment shown in Figures 5-7.

Referring to Figure 15, planarization can be conducted (i.e., chemical-mechanical polishing) to remove layers 44, 22, 21 and 20 from over substrate 12 outside of trenches 14.

Alternatively, the silanol 44 could be formed within trenches 14 and converted before a sidewall oxidation. Preferably in such instance, the thermal oxidation conditions comprise flowing an oxidizing gas at 200 sccm (i.e., O_2, O_3, N_2O, NO_X or any mixture combination thereof) over substrate 12 within trenches 14 while substrate 12 is maintained at from 850°C to 1150°C and reactor pressure at from 10 Torr to 760 Torr for from 5 to 30 minutes.

Further in accordance with the invention, sidewalls 16 might be oxidized prior to forming first layer 26 in the first embodiment, or prior to forming first layer 40 in the second embodiment. Alternately, sidewalls 16 might be oxidized after forming first layer 26 and before forming second layer 30 in the first embodiment, or after forming first layer 40 and before forming second layer 44 in the second embodiment or after forming layer 50 and before forming layer 30 in the third embodiment. Further alternately, sidewalls 16 might be oxidized after forming second layer 30 in the first embodiment, or after forming layer 44 in the second embodiment. Further alternately with respect to the third embodiment, and where layer 21 is not formed by thermal

oxidation, the sidewalls might be oxidized after forming layer 50 and before forming layer 30, or after forming layer 50. Conventional thermal oxidations are preferably conducted in such instances.

In the preferred first embodiment, first layer 26 flows conformably into the trenches during deposition without forming any constrictions at the top of the trenches where voids begin. The first layer 26 effectively lowers the aspect ratio (defined as trench depth to width) of the trenches preferably by filling at least about a third of the depth while only adding at most 200 angstroms of layer on the sidewalls. As a result, any subsequent layer deposited to fill the layer will have a trench with a lower aspect ratio more conducive to filling without voids.

In the less preferred second and third embodiments, the first layer is formed by less preferred methods which may not lower the aspect ratio as significantly as in the first embodiment.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.